cont. A1 achieving lower resistance. - -

IN THE CLAIMS:

Please amend the claims to read as follows:

sub B2 5. (Amended) A method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements, said method comprising:

forming a metal film directly on surfaces of source-drain regions and gate regions in said DRAM section and said logic section; and

A2 heat treating said device to react said metal film with said surfaces to form a metal silicide layer.

6. (Amended) The method of manufacturing a semiconductor device according to Claim 5, wherein said metal film is formed over an entire surface of said substrate, and wherein said heat treating removes unreacted metal film.

9. (Amended) The method of manufacturing a semiconductor device according to Claim 5, further comprising:

A3 forming a bit contact connecting said DRAM section with a bit line and a contact plug connecting to said source-drain in said logic section, said bit contact and said contact plug comprising a metal material.

sub B3 12. (Amended) A method of manufacturing a semiconductor device having a memory cell section and an adjacent circuit section, said method comprising:

forming a metal film directly on surfaces of source-drain regions and gate regions in said memory cell section and said adjacent circuit section; and

A4 annealing said device to react said metal film with said surfaces to form a metal silicide layer.

13. (Amended) The method of manufacturing a semiconductor device according to Claim 12, wherein said forming a metal film comprises forming a metal film over an entire surface

cont. A4

of said substrate, and wherein said heat treating removes unreacted metal film.

Please add the following new claims:

Sub B4

- - 15. A method of manufacturing a semiconductor device comprising:

forming a metal film on source-drain and gate surfaces in a memory cell section of a substrate, and on source-drain and gate surfaces in an adjacent circuit section of said substrate; and

heat treating said device to react said metal film with silicon in said surfaces to form a metal silicide layer.

16. The method of manufacturing a semiconductor device according to Claim 12, wherein said forming a metal film comprises a sputtering method. 103

17. The method of manufacturing a semiconductor device according to Claim 12, wherein said heat treating comprises heating said device at 500-600 °C in a nitrogen atmosphere for 30 seconds, and heating said device at 800 °C in a nitrogen atmosphere for 10 seconds. 103

A5

18. The method of manufacturing a semiconductor device according to Claim 12, wherein said source-drain regions in said memory cell section comprise a high dopant concentration.

19. The method of manufacturing a semiconductor device according to Claim 12, further comprising:

forming an ohmic contact on said silicide layer on a source-drain region. 112, 1, ¶ 2 103

20. The method of manufacturing a semiconductor device according to Claim 12, further comprising:

forming source-drain regions in said memory cell section and said adjacent circuit section.

21. The method of manufacturing a semiconductor device according to Claim 20, wherein said forming source-drain regions comprises implanting BF_2 ions in a source-drain region at a 103

concentration of 3 x 10^{15}/ cm^3.

Cont, A5 22. The method of manufacturing a semiconductor device according to Claim 20, wherein said forming source-drain regions comprises implanting Aresenic ions in a source-drain region at a concentration of 6 x 10^{15}/ cm^3. - - 123